IN THE CLAIMS

1. (original) A digital signal processor comprising:

a first data classification block (DCB) that outputs a first block priority number (BPN) associated with a first data stored in the first DCB that matches a search key;

a second DCB that outputs a second BPN associated with a second data stored in the second DCB that matches the search key; and

a device index processor that determines a most significant block priority number (MSBPN) from the first BPN and the second BPN.

2. (original) The digital signal processor of claim 1, wherein the device index processor outputs a device index for data associated with the MSBPN.

3. (original) The digital signal processor of claim 1, wherein the first DCB outputs a first block index associated with the first data, and the second DCB outputs a second block index associated with the second data.

4. (original) The digital signal processor of claim 3, wherein the device index processor comprises:

a compare logic that determines the MSBPN from the first BPN and the second BPN; and

an inhibit signal generator that outputs enable signals that indicate which DCBs originate the MSBPN.

5. (original) The digital signal processor of claim 4, wherein the inhibit signal generator comprises a plurality of comparator circuits.

6. (original) The digital signal processor of claim 4, wherein the first DCB outputs a first match flag signal that indicates whether the MSBPN originates from the first DCB, and the second DCB outputs a second match flag signal that indicates whether the

MSBPN originates from the second DCB.

7. (original) The digital signal processor of claim 4, wherein each of the first and second DCBs comprises:

a data table that stores data;

a priority memory that stores a plurality of priority numbers, each priority number associated with a corresponding data in the data table and indicating a priority of the corresponding data relative to other data in the data table;

a priority logic that compares priority numbers in the priority memory associated with data in the data table that match the search key and provides an indication of a most significant priority number as a BPN for the DCB on a match line segment;

a row enable logic that propagates the indication of the BPN on the match line segment in response to receiving the enable signal;

a match flag generator that outputs a match flag signal that indicates whether the BPN for the DCB is the MSBPN in response to the row enable logic propagating the indication; and

an encoder that generates an index relative to the DCB associated with the indication propagated by the row enable logic.

8. (original) The digital signal processor of claim 7, wherein the row enable logic comprises a plurality of circuits that perform an AND function.

9. (original) The digital signal processor of claim 7, wherein the match flag generator comprises a circuit that performs an OR function.

10. (original) The digital signal processor of claim 6, wherein the device index processor further comprises an address generator that determines a device index from the first and second block indices and the first and second match flag signals.

11. (original) The digital signal processor of claim 10, wherein the address generator

comprises a priority encoder that outputs a block identifier that identifies a DCB that originates the MSBPN, and when both the first and second DCBs originate the MSBPN, the priority encoder outputs a block identifier corresponding to a DCB that has a higher priority.

12. (original) The digital signal processor of claim 11, wherein the address generator further comprises an index storage unit that includes:

a first storage element, having a first address, that stores the first block index; and

a second storage element, having a second address, that stores the second block index.

13. (original) The digital signal processor of claim 12, wherein the address generator further comprises a decoder that decodes the block identifier output from the priority encoder into an address of a storage element that stores a block index output from a data classification block corresponding to the block identifier.

14. (original) The digital signal processor of claim 11, wherein the address generator further comprises a multiplexer that receives the first and second block indices.

15. (original) The digital signal processor of claim 14, wherein the address generator further comprises a decoder that decodes the block identifier output from the priority encoder and selects one of the first and second block indices to be output from the multiplexer in response to the block identifier.

16. (original) The digital signal processor of claim 15, further comprising an index generator that outputs the device index for data associated with the MSBPN, the index generator designating the block identifier output from the priority encoder as the most significant bits of the device index and a block index output from the multiplexer as the least significant bits of the device index.

17. (original) The digital signal processor of claim 4, wherein the compare logic includes:

a first compare logic circuit that determines a first most significant sub-block priority number (MSSBPN) from a first sub-block priority number (SBPN) from the first DCB and a SBPN from the second DCB, and that outputs first compare logic circuit control signals that indicate which DCB originates the first MSSBPN; and

a second compare logic circuit that determines a second MSSBPN from a second SBPN from the first DCB and a second SBPN from the second DCB, and that outputs second compare logic circuit control signals that indicate which DCB originates the first and second MSSBPNs, where each of the second SBPN from the first and second DCBs is assigned a least significant sub-block priority number (LSSBPN) if the first MSSBPN did not originate from its DCB.

18. (original) The digital signal processor of claim 17, wherein the first compare logic circuit comprises:

a first stage comparator for the first compare logic circuit that compares the first SBPNs from the first and second DCBs to determine the first MSSBPN;

a first second stage comparator for the first compare logic circuit that compares the first MSSBPN with the first SBPN from the first DCB and that generates a first control signal that indicates whether the first MSSBPN originates from the first DCB; and

a second second stage comparator for the first compare logic circuit that compares the first MSSBPN with the first SBPN from the second DCB and that generates a second control signal that indicates whether the first MSSBPN originates from the second DCB.

19. (original) The digital signal processor of claim 18, wherein the first and second second stage comparators each comprises a plurality of circuits that perform an XNOR function with outputs coupled to a circuit that performs an AND function.

20. (original) The digital signal processor of claim 18, wherein the second compare logic circuit comprises:

a compare enable circuit that assigns a LSSBPN to the second SBPN from the first DCB upon receiving a first control signal that indicates that the first MSSBPN did not originate from the first DCB, and that assigns a LSSBPN to the second SBPN from the second DCB upon receiving a second control signal that indicates that the first MSSBPN did not originate from the second DCB;

a first stage comparator for the second compare logic circuit that compares the second SBPNs from the first and second DCBs to determine the second MSSBPN;

a first second stage comparator for the second compare logic circuit that compares the second MSSBPN with the second SBPN from the first DCB and that generates a first output that indicates whether there is a match; and

a second second stage comparator for the second compare logic circuit that compares the second MSSBPN with the second SBPN from the second DCB and that generates a second output that indicates whether there is a match.

21. (original) The digital signal processor of claim 20, wherein the second compare logic further comprises:

a first control signal processor that receives the first control signal and the first output and that generates a third control signal that indicates whether the first and second MSSBPNs originate from the first DCB; and

a second control signal processor that receives the second control signal and the second output and that generates a fourth control signal that indicates whether the first and second MSSBPNs originate from the second DCB.

22. (currently amended) The digital signal processor of claim ~~2321~~, wherein each of the first and second control signal processors comprises a circuit that performs an OR function.

23. (original) The digital signal processor of claim 17, wherein the compare logic further comprises a third compare logic circuit that determines a third MSSBPN from a third SBPN from the first DCB and a third SBPN from the second DCB, and that outputs third compare logic circuit control signals that indicate which DCB originates the first, second, and third MSSBPNs, where each of the third SBPNs from the first and second DCBs is assigned the LSBPN if the first and second MSSBPNs did not originate from its DCB.

24. (original) The digital signal processor of claim 23, wherein the third compare logic circuit control signals are transmitted to the first and second DCBs as enable signals that indicate whether a DCB originates the MSBPN.

25. (original) The digital signal processor of claim 17, wherein the first compare logic circuit comprises a first priority index table and the second compare logic circuit comprises a second priority index table.

26. (original) The digital signal processor of claim 1, wherein the DCB stores Internet Protocol addresses and the first and second BPNs comprise prefix mask data for the Internet Protocol addresses.

27. (original) The digital signal processor of claim 1, wherein the DCB stores policy statements and the first and second BPNs indicate the relative priority of the policy statements.

28. (original) The digital signal processor of claim 1, wherein the DCB includes a content addressable memory (CAM) array.

29. (original) A method for processing data, comprising:

determining a first block priority number from a first plurality of priority numbers where each of the first plurality of priority numbers are associated with data stored in a

first data classification block (DCB) that matches a search key;

determining a second block priority number from a second plurality of priority numbers where each of the second plurality of priority numbers are associated with data stored in a second DCB that match the search key; and

determining a most significant block priority number (MSBPN) from the first block priority number and the second block priority number.

30. (original) The method of claim 29, further comprising generating a device index of data associated with the most significant priority number.

31. (original) The method of claim 29, further comprising:

determining a first block index associated with the first block priority number; and

determining a second block index associated with the second block priority number.

32. (original) The method of claim 31, further comprising:

determining which of the first and second data classification blocks originates the MSBPN; and

transmitting enable signals to the first and second DCBs that indicate whether a DCB originates the MSBPN.

33. (original) The method of claim 32, further comprising:

generating a first match flag signal that indicates whether the MSBPN originates from the first DCB; and

generating a second match flag signal that indicates whether the MSBPN originates from the second DCB.

34. (original) The method of claim 33, further comprising:

storing the first block index in a first storage element having a first address; and

storing the second block index in a second storage element having a second address.

35. (original) The method of claim 34, further comprising:

encoding a match flag signal received into a most significant block identifier;

decoding the most significant block identifier into an address of a storage element that stores a block index output from a data classification block corresponding to the most significant block index;

outputting a most significant block index in response to asserting the address; and

generating a device index from the most significant block identifier and the most significant block index.

36. (original) The method of claim 35, wherein generating the device index comprises:

designating the most significant block identifier as most significant bits of a device index; and

designating the most significant block index as least significant bits of the device index.

37. (original) The method of claim 32, wherein the first and second block priority numbers comprise a plurality of sub-block priority numbers (SBPN).

38. (original) The method of claim 37, wherein determining which of the first and second DCBs originates the MSBPN comprises:

determining a first most significant sub-block priority number (MSSBPN) from a first SBPN from the first DCB and a first SBPN from the second DCB and outputting first compare logic circuit control signals that indicate which DCB originates the first MSSBPN; and

determining a second MSSBPN from a second SBPN from the first DCB and a second SBPN from the second DCB, where each of the second SBPN from the first and second DCBs is assigned a least significant sub-block priority number (LSSBPN) if the first MSSBPN did not originate from its DCB, and outputting second compare logic

circuit control signals that indicate which DCB originates the first and second MSSBPNs.

39. (original) The method of claim 38, wherein determining which of the first and second DCBs originates the MSBPN further comprises determining a third MSSBPN from a third SBPN from the first DCB and a third SBPN from the second DCB, where each of the third SBPNs from the first and second DCBs is assigned the LSBPN if the first and second MSSBPNs did not originate from its DCB, and outputting third compare logic circuit control signals that indicate which DCB originate the first, second, and third MSSBPN, where the DCB that originates the third MSSBPN is the DCB that originates the MSBPN.

40. (original) The method of claim 39, further comprising transmitting the third compare logic control signals as enable signals to the first and second DCBs that indicate whether the MSBPN originates from it.

41. (original) The method of claim 38, wherein determining the first MSSBPN and outputting first compare logic circuit control signal comprises:

comparing the first SBPNs from the first and second DCBs to determine the MSSBPN;

comparing the first MSSBPN with the first SBPN from the first DCB;

generating a first control signal that indicates whether the first MSSBPN originates from the first DCB;

comparing the first MSSBPN with the first SBPN from the second DCB; and generating a second control signal that indicates whether the first MSSBPN originates from the second DCB.

42. (original) The method of claim 41, wherein determining the second MSSBPN and outputting second compare logic circuit control signal comprises:

assigning a LSSBPN to a second SBPN from the first DCB upon receiving the first

control signal indicating that the first MSSBPN did not originate from the first DCB;

assigning a LSSBPN to a second SBPN from the second DCB upon receiving the second control signal indicating that the first MSSBPN did not originate from the second DCB;

comparing the second SBPNs from the first and second DCBs to determine the second MSSBPN;

comparing the second MSSBPN with the second SBPN from the first DCB and generating a first output that indicates whether or not there was a match; and

comparing the second MSSBPN with the second SBPN from the second DCB and generating a second output that indicates whether or not there was a match.

43. (original) The method of claim 42, wherein determining the second MSSBPN and outputting second compare logic circuit control signal further comprises:

performing an OR function on the first control signal and the first output; and

performing an OR function on the second control signal and the second output.

44. (original) A digital signal processor comprising:

means for determining a first block priority number (BPN) associated with a first data stored in a first data classification block (DCB) that matches a search key;

means for determining a second BPN associated with a second data stored in a second DCB that matches the search key; and

means for determining a most significant block priority number (MSBPN) from the first BPN and the second BPN.

45. (original) The digital signal processor of claim 44, wherein the means for determining the first block priority number determines a first block index associated with the first data, and the means for determining the second priority number determines a second block index associated with the second data.

46. (original) The digital signal processor of claim 45, wherein the means for determining the MSBPN comprises:

means for determining the MSBPN from the first BPN and the second BPN; and means for determining enable signals that indicate which DCBs originate the MSBPN.

47. (original) The digital signal processor of claim 46, wherein the means for determining the first BPN determines a first match flag signal that indicates whether the MSBPN originates from the first DCB and the means for determining the second BPN determines a second match flag signal that indicates whether the MSBPN originates from the DCB.

48. (original) The digital signal processor of claim 47, wherein the means for determining the MSBPN further comprises a means for determining a device index from the first and second block indices and the first and second match flag signals.

49. (original) The digital signal processor of claim 46, wherein the means for determining the MSBPN from the first BPN and the second BPN includes:

means for determining a first most significant sub-block priority number (MSSBPN) from a first sub-block priority number (SBPN) from the first DCB and a SBPN from the second DCB, and that outputs first compare logic circuit control signals that indicate which DCB originates the first MSSBPN; and

means for determining a second MSSBPN from a second SBPN from the first DCB and a second SBPN from the second DCB, and that outputs second compare logic circuit control signals that indicate which DCB originates the first and second MSSBPNs, where each of the second SBPN from the first and second DCBs is assigned a least significant sub-block priority number (LSSBPN) if the first MSSBPN did not originate from its DCB.

50. (original) A digital signal processor, comprising:

a plurality of data classification blocks each comprising:

a data table that stores uniquely addressable data entries;

a priority index table coupled to the data table;

a row enable logic circuit coupled to the priority index table;

a match flag signal generator coupled to the row enable logic circuit;

an encoder coupled to the row enable encoder circuit; and

a device index processor coupled to the plurality of priority index tables, match flag signal generators, and row enable encoder circuits to determine the index for at least one of the data entries that matches a search key.

51. (original) The digital signal processor of claim 50, wherein each priority index table comprises:

memory that stores priority numbers for each corresponding data entry; and

compare logic that determine a most significant priority number for the data classification block.

52. (original) The digital signal processor of claim 50, wherein each row enable logic circuit comprises circuitry that processes signals on internal address lines from the priority index table and an enable signal from the device index processor.

53. (original) The digital signal processor of claim 50, wherein each match flag signal generator comprises circuitry that processes signals on internal address lines from the row enable logic circuit.

54. (original) The digital signal processor of claim 50, wherein the device index processor comprises:

a compare logic;

an inhibit signal generator coupled to the compare logic; and

a device index generator coupled to the plurality of data classification blocks.